# DATA SHEET

# TDA8758
## YC 8-bit low-power analog-to-digital video interface

Product specification
Supersedes data of 1995 Mar 22
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

# YC 8-bit low-power analog-to-digital video interface

# TDA8758

## FEATURES

- Two 8-bit ADCs:
  - one Luminance or CVBS channel
  - one Chrominance channel
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs for each channel
- Internal reference voltage regulator
- TTL-compatible digital inputs and outputs
- Power dissipation of 530 mW (typical)
- Input selector circuit (five selectable video inputs for CVBS or YC processing)
- Peak white enable input
- Clamp and Automatic Gain Control (AGC) functions for Y/CVBS channel (clamping on code 64 and Peak White level control at code 255)
- Clamp function for C channel (code 128)
- No sample-and-hold circuit required.

## APPLICATIONS

- Video signal decoding
- Digital picture processing
- Frame grabbing
- Multimedia with the Philips Desktop Video chip set (and especially SAA7196 multistandard decoder and scaler).

## GENERAL DESCRIPTION

The TDA8758 is an 8-bit video high-speed low-power analog-to-digital conversion (ADC) interface for YC and CVBS signal processing. It converts 1-of-3 CVBS input signals or 1-of-2 YC input signals into binary or two's complement words at a sampling rate of 32 MHz.
All analog signal inputs are digitally clamped and an ADC interface is provided on the Y/CVBS channel. A fast precharge on clamp and AGC is provided for start-up.
All digital inputs and outputs are TTL compatible.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCD}$ | digital supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCO}$ | output stages supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $I_{CCA}$ | analog supply current | | – | 59 | 70 | mA |
| $I_{CCD}$ | digital supply current | | – | 28 | 40 | mA |
| $I_{CCO}$ | output supply current | $C_L$ = 15 pF | – | 19 | 28 | mA |
| ILE | DC integral linearity error | | – | ±0.75 | ±1.5 | LSB |
| DLE | DC differential linearity error | | – | ±0.4 | ±1.0 | LSB |
| EB | effective bits (from video input to digital outputs) | $f_{clk}$ = 32 MHz; $f_i$ = 4.43 MHz | – | 7.1 | – | bits |
| $f_{clk(max)}$ | maximum clock frequency | | 30 | 32 | – | MHz |
| B | maximum –3 dB bandwidth (input preamplifier) | full-scale; 0 dB gain | – | 15 | – | MHz |
| $\alpha_{ct}$ | crosstalk between Y and C channels and each video input | | – | –63 | –55 | dB |
| $P_{tot}$ | total power dissipation | | – | 530 | 724 | mW |

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TDA8758G | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |

## BLOCK DIAGRAM

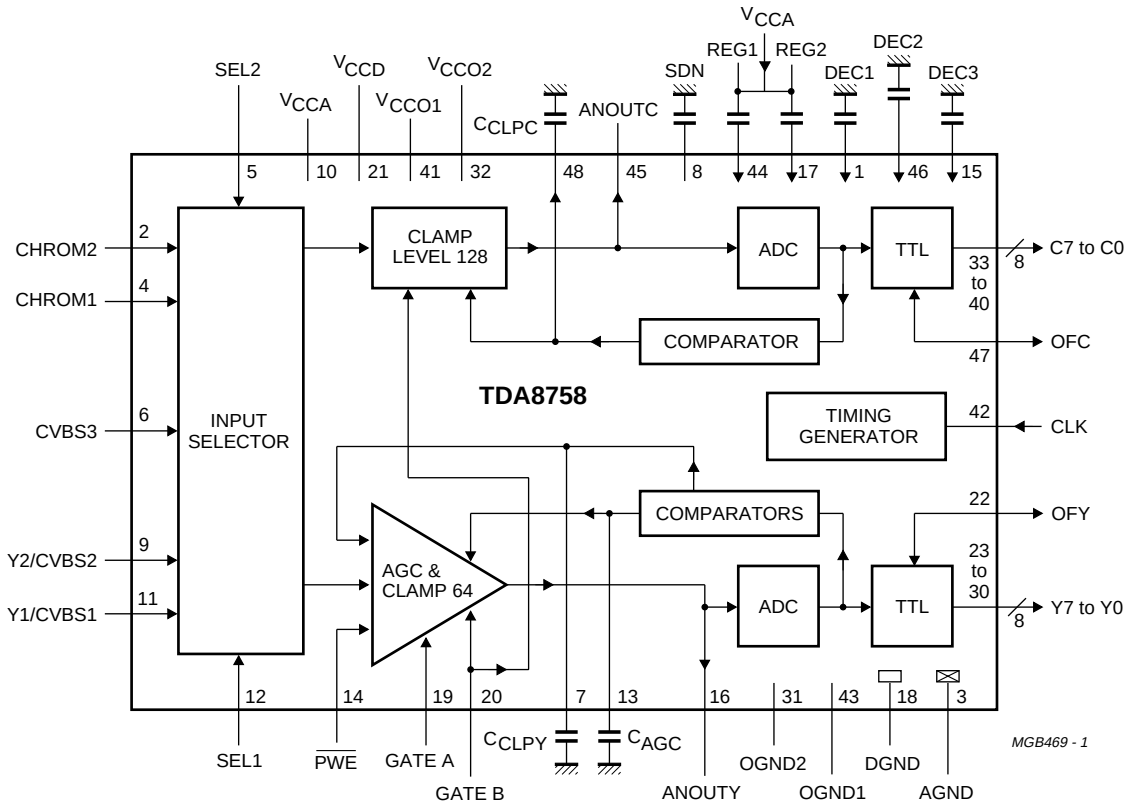



Fig.1 Block diagram.

**PINNING**

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| DEC1 | 1 | decoupling input 1 |
| CHROM2 | 2 | chrominance analog voltage input 2 |
| AGND | 3 | analog ground |
| CHROM1 | 4 | chrominance analog voltage input 1 |
| SEL2 | 5 | selection control input 2 |
| CVBS3 | 6 | luminance analog voltage input 3 |
| $C_{CLPY}$ | 7 | Y channel clamping capacitor |
| SDN | 8 | stabilizer decoupling node |
| Y2/CVBS2 | 9 | luminance analog voltage input 2 |
| $V_{CCA}$ | 10 | analog supply voltage (+5 V) |
| Y1/CVBS1 | 11 | luminance analog voltage input 1 |
| SEL1 | 12 | selection control input 1 |
| $C_{AGC}$ | 13 | AGC capacitor |
| $\overline{PWE}$ | 14 | peak white enable input (active LOW) |
| DEC3 | 15 | decoupling input 3 |
| ANOUTY | 16 | analog output for Y channel |
| REG2 | 17 | decoupling input 2 (internal stabilization loop decoupling) |
| DGND | 18 | digital ground |
| GATE A | 19 | AGC control input |
| GATE B | 20 | clamp control input |
| $V_{CCD}$ | 21 | digital supply voltage (+5 V) |
| OFY | 22 | Y channel output format/chip enable (3-state input) |
| Y7 | 23 | Y channel data output; bit 7 (MSB) |
| Y6 | 24 | Y channel data output; bit 6 |
| Y5 | 25 | Y channel data output; bit 5 |
| Y4 | 26 | Y channel data output; bit 4 |
| Y3 | 27 | Y channel data output; bit 3 |
| Y2 | 28 | Y channel data output; bit 2 |
| Y1 | 29 | Y channel data output; bit 1 |
| Y0 | 30 | Y channel data output; bit 0 (LSB) |
| OGND2 | 31 | output ground 2 |
| $V_{CCO2}$ | 32 | output supply voltage 2 (+5 V) |
| C7 | 33 | C channel data output; bit 7 (MSB) |
| C6 | 34 | C channel data output; bit 6 |
| C5 | 35 | C channel data output; bit 5 |
| C4 | 36 | C channel data output; bit 4 |
| C3 | 37 | C channel data output; bit 3 |
| C2 | 38 | C channel data output; bit 2 |
| C1 | 39 | C channel data output; bit 1 |
| C0 | 40 | C channel data output; bit 0 (LSB) |

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| $V_{CCO1}$ | 41 | output supply voltage 1 (+5 V) |
| CLK | 42 | clock input |
| OGND1 | 43 | output ground 1 |
| REG1 | 44 | decoupling input 1 (internal stabilization loop decoupling) |
| ANOUTC | 45 | analog output for C channel |
| DEC2 | 46 | decoupling input 2 |
| OFC | 47 | C channel output format/chip enable (3-state input) |
| $C_{CLPC}$ | 48 | C channel clamping capacitor |

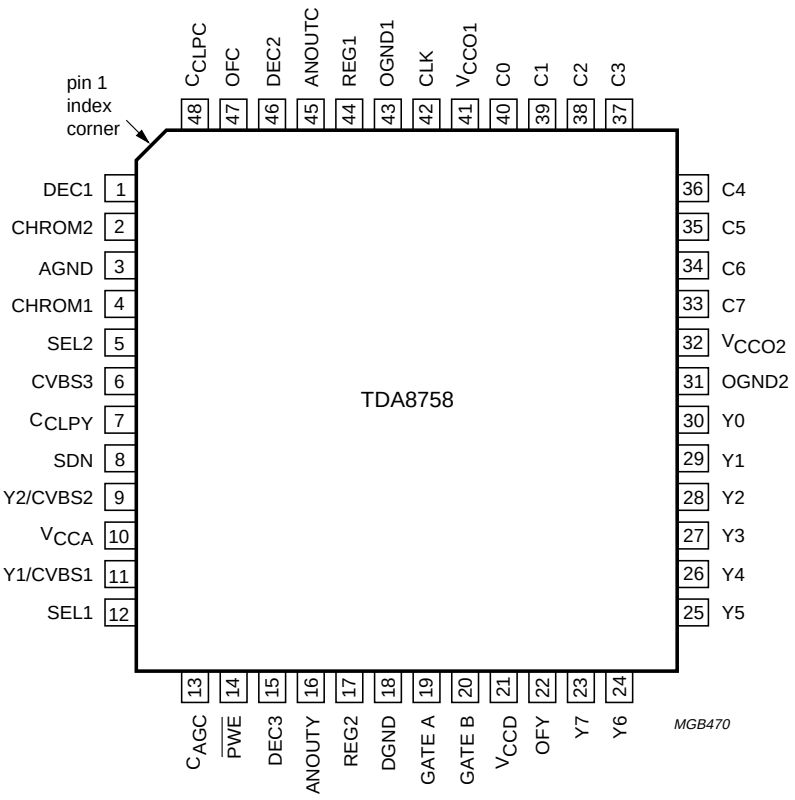



Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

The TDA8758 provides a simple interface between CVBS or Y/C analog signals and a digital colour decoder.

### Video inputs selection

The input selector allows a choice from different video sources, and has one of the following configurations:

A: Two Y/C and one CVBS signals

B: One Y/C and two CVBS signals

C: Three CVBS signals (only the Y channel is used).

The wiring of the five video inputs (pins 2, 4, 6, 9 and 11) and the control of the two selection inputs (pins 5 and 12) will depend on the available video sources.

- In configuration A, connect as follows:
  - Y1 to pin 11
  - C1 to pin 4
  - Y2 to pin 9
  - C2 to pin 2
  - CVBS3 to pin 6.

  Keep SEL2 (pin 5) LOW and select Y1/C1 or Y2/C2 by switching SEL1 (pin 12).

  CVBS3 is selected with SEL1 and SEL2 HIGH.
- In configuration B, replace Y1 (or Y2) by a CVBS input (no more C1 or C2). The selection mode is the same.
- In configuration C, connect as follows:
  - CVBS1 to pin 11
  - CVBS2 to pin 9
  - CVBS3 to pin 6.

  Use both SEL1 and SEL2 to select inputs.

**Remark**: the video inputs selection is a static selection.

### Synchronization pulses

GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively. They should be distinct.

On the Y channel, the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the $C_{AGC}$ pin. The voltage across this capacitor controls the gain of the video amplifier. This is the control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 1 at the converter Y output. As the black level is digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The Peak White control loop is active when the selection pin $\overline{PWE}$ is LOW. Then, if the Y video signal exceeds the digital code of 255, it will be limited to avoid any over-range of the converter.

The clamp level control is accomplished by using the same techniques as used for the gain control. On both Y and C channels, the black level digital comparators are active during a positive-going pulse at the GATE B input. On the Y channel, the clamping capacitor connected to the $C_{CLPY}$ pin will be charged or discharged to adjust the digital output to code 64. On the C channel, the clamping capacitor connected to the $C_{CLPC}$ pin will be charged or discharged to adjust the digital output to code 128.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | | –0.3 | +7.0 | V |
| $V_{CCD}$ | digital supply voltage | | –0.3 | +7.0 | V |
| $V_{CCO}$ | output supply voltage | | –0.3 | +7.0 | V |
| $\Delta V_{CC}$ | supply voltage difference between $V_{CCA}$ and $V_{CCD}$ | | –1.0 | +1.0 | V |
| | supply voltage difference between $V_{CCO}$ and $V_{CCD}$ | | –1.0 | +1.0 | V |
| | supply voltage difference between $V_{CCA}$ and $V_{CCO}$ | | –1.0 | +1.0 | V |
| $V_I$ | input voltage | referenced to AGND | – | 5.0 | V |
| $V_{clk(p-p)}$ | AC input voltage for switching (peak-to-peak value) | referenced to DGND | – | $V_{CCO}$ | V |
| $I_O$ | output current | | – | +6 | mA |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_{amb}$ | operating ambient temperature | | 0 | +70 | °C |
| $T_j$ | junction temperature | | – | +150 | °C |

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---|---|---|---|
| $R_{th\ j\text{-}a}$ | thermal resistance from junction to ambient in free air | 72 | K/W |

## CHARACTERISTICS

$V_{CCA} = V_{10}$ to $V_3$ = 4.75 to 5.25 V; $V_{CCD} = V_{21}$ to $V_{18}$ = 4.75 to 5.25 V; $V_{CCO1} = V_{41}$ to $V_{43}$ = 4.75 to 5.25 V; $V_{CC02} = V_{32}$ to $V_{31}$ = 4.75 to 5.25 V; AGND and DGND shorted together; $V_{CCA}$ to $V_{CCD}$ = –0.25 to +0.25 V; $V_{CCO}$ to $V_{CCD}$ = –0.25 to +0.25 V; $V_{CCA}$ to $V_{CCO}$ = –0.25 to +0.25 V; $T_{amb}$ = 0 to +70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and $T_{amb}$ = 25 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{CCA}$ | analog supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCD}$ | digital supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCO}$ | output stages supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $I_{CCA}$ | analog supply current | | – | 59 | 70 | mA |
| $I_{CCD}$ | digital supply current | | – | 28 | 40 | mA |
| $I_{CCOtot}$ | total output supply current | $C_L$ = 15 pF | – | 19 | 28 | mA |
| **Video amplifier inputs** | | | | | | |
| Y1/CVBS1, Y2/CVBS2, CVBS3, CHROM1 AND CHROM2 INPUTS | | | | | | |
| $V_{I(p-p)}$ | input voltage (peak-to-peak value) | AGC load with external capacitor; note 1 | | | | |
| | Y channel | | 0.7 | – | 1.4 | V |
| | C channel | | – | 1.0 | – | V |
| $\|Z_i\|$ | input impedance | $f_i$ = 6 MHz | – | 25 | – | kΩ |
| $C_I$ | input capacitance | $f_i$ = 6 MHz | – | 2 | – | pF |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| SEL1 AND SEL2 TTL INPUTS; see Table 1 | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW level input current | $V_I$ = 0.4 V | –400 | – | – | μA |
| $I_{IH}$ | HIGH level input current | $V_I$ = 2.7 V | – | – | 20 | μA |
| GATE A AND GATE B TTL INPUTS; see Figs 5 and 6 | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW level input current | $V_I$ = 0.4 V | –400 | – | – | μA |
| $I_{IH}$ | HIGH level input current | $V_I$ = 2.7 V | – | – | 20 | μA |
| AGC INPUT (PIN 13); see Fig.8 | | | | | | |
| $V_{13(min)}$ | AGC voltage for minimum gain at –3 dB | | – | 3.3 | – | V |
| $V_{13(max)}$ | AGC voltage for maximum gain at +3 dB | | – | 3.75 | – | V |
| $I_{12}$ | AGC output current | | see Table 2 | | | |
| C-CHANNEL CLAMP INPUT (PIN 48) | | | | | | |
| $V_{48}$ | CLAMP voltage for code 128 output | | – | 3.45 | – | V |
| $I_{48}$ | CLAMP output current | | see Table 3 | | | |
| Y-CHANNEL CLAMP INPUT (PIN 7) | | | | | | |
| $V_7$ | CLAMP voltage for code 64 output | | – | 3.70 | – | V |
| $I_7$ | CLAMP output current | | see Table 3 | | | |
| **Video amplifier dynamic characteristics** | | | | | | |
| $\alpha_{ct}$ | crosstalk between video inputs (pins 2, 4, 6, 9 and 11) | $V_{CCA}$ = 4.75 to 5.25 V | – | –63 | –55 | dB |
| B | –3 dB bandwidth | | – | 15 | – | MHz |
| ΔG | gain range | | –3 | – | +3 | dB |
| $G_{stab}$ | gain stability as a function of: | | | | | |
| | supply voltage | $f_i$ = 4.43 MHz | – | – | 0.5 | % |
| | supply voltage and temperature | | – | – | 6 | % |
| **Analog-to-digital converter inputs** | | | | | | |
| CLK INPUT (PIN 42) | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW level input current | $V_{clk}$ = 0.4 V | –400 | – | – | μA |
| $I_{IH}$ | HIGH level input current | $V_{clk}$ = 2.7 V | – | – | 20 | μA |
| $C_I$ | input capacitance | $f_{clk}$ = 32 MHz | – | 2 | – | pF |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| OFY AND OFC INPUTS; 3-STATE; see Table 4 | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.2 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.6 | – | $V_{CCD}$ | V |
| $V_I$ | input voltage in high impedance state | | – | 1.15 | – | V |
| $I_{IL}$ | LOW level input current | | –370 | –300 | – | μA |
| $I_{IH}$ | HIGH level input current | | – | 500 | 700 | μA |
| **Analog-to-digital converter outputs** | | | | | | |
| ANOUTY AND ANOUTC OUTPUTS (PINS 16 AND 45); see Table 5 | | | | | | |
| $V_{ANOUT}$ | output voltage | digital output = 00 | – | 2.6 | – | V |
| $V_{ANOUT}$ | output voltage | digital output = 255 | – | 3.6 | – | V |
| $V_{ANOUT(p-p)}$ | output voltage amplitude (peak-to-peak value) | | – | 1.0 | – | V |
| DIGITAL OUTPUTS Y0 TO Y7, C0 TO C7 | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_{OL}$ = 2 mA | 0 | – | 0.6 | V |
| $V_{OH}$ | HIGH level output voltage | $I_{OL}$ = –0.4 mA | 2.4 | – | $V_{CCD}$ | V |
| **Switching characteristics;** see Fig.9 | | | | | | |
| $f_{clk(max)}$ | CLK input maximum frequency | note 2 | 30 | 32 | – | MHz |
| $t_{CPH}$ | clock pulse width HIGH | | 12 | – | – | ns |
| $t_{CPL}$ | clock pulse with LOW | | 12 | – | – | ns |
| **Analog signal processing from video input to digital output on both channels; 0 dB gain ($f_{clk}$ = 32 MHz)** | | | | | | |
| INL | DC integral non-linearity | | – | ±0.75 | ±1.5 | LSB |
| DNL | DC differential non-linearity | | – | ±0.4 | ±1.0 | LSB |
| AINL | AC integral non linearity | $f_i$ = 4.43 MHz | – | ±1.5 | – | LSB |
| ADNL | AC differential non-linearity | $f_i$ = 4.43 MHz | – | ±0.5 | – | LSB |
| THD | total harmonic distortion | note 3 | – | –52 | – | dB |
| EB | effective bits | $f_i$ = 4.43 MHz; note 4 | – | 7.1 | – | bits |
| $G_{diff}$ | differential gain | $V_{16,45}$ = 1.0 V (p-p); see Fig.4; PAL modulated ramp; note 5 | – | 1.5 | 3.0 | % |
| $\varphi_{diff}$ | differential phase | see Fig.5; PAL modulated ramp; note 5 | – | 0.6 | 1.5 | deg |
| SVRR2 | supply voltage ripple rejection | note 6 | – | – | 5 | %/V |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Timing ($f_{clk}$ = 32 MHz);** see Fig.9 | | | | | | |
| DIGITAL OUTPUTS ($C_L$ = 15 pF) | | | | | | |
| $t_{ds}$ | sampling delay time | | – | 2 | – | ns |
| $t_h$ | output hold time | | 10 | – | – | ns |
| $t_d$ | output delay time | | – | 15 | 18 | ns |
| $t_W$ | clamp pulse width | see Figs 6 and 7 | 2 | 3 | – | μs |
| **3-state output delay times;** see Fig.10 | | | | | | |
| $t_{dZH}$ | enable HIGH | | – | 12 | 14 | ns |
| $t_{dZL}$ | enable LOW | | – | 10 | 12 | ns |
| $t_{dHZ}$ | disable HIGH | | – | 58 | 62 | ns |
| $t_{dLZ}$ | disable LOW | | – | 70 | 74 | ns |

**Notes**

1. 0 dB is obtained at the AGC amplifier when applying $V_{I(p\text{-}p)}$ = 1.0 V on Y channel.
2. It is recommended that the rise and fall times of the clock are ≥1 ns. In addition, a ‘good layout’ for the digital and analog grounds is recommended.
3. THD (total harmonic distortion) is obtained with the addition of the first five harmonics:

$$THD = 20 \log \frac{F}{\sqrt{(2nd)^2 + (3rd)^2 + (4th)^2 + (5th)^2 + (6th)^2}}$$

   a) F being the fundamental harmonic referenced at 0 dB for a full-scale sine wave input.
4. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8 K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
5. Measurement carried out using video analyser VM700A, where video analog signal is reconstructed through a digital-to-analog converter.
6. The supply voltage ripple rejection is the relative variation of the analog signal (full-scale signal at input) for 0.5 V of supply variation:

$$SVRR2 = \frac{\Delta (V_{I(00)} - V_{I(FF)}) \times (V_{I(00)} - V_{I(FF)})}{\Delta V_{CCA}}$$

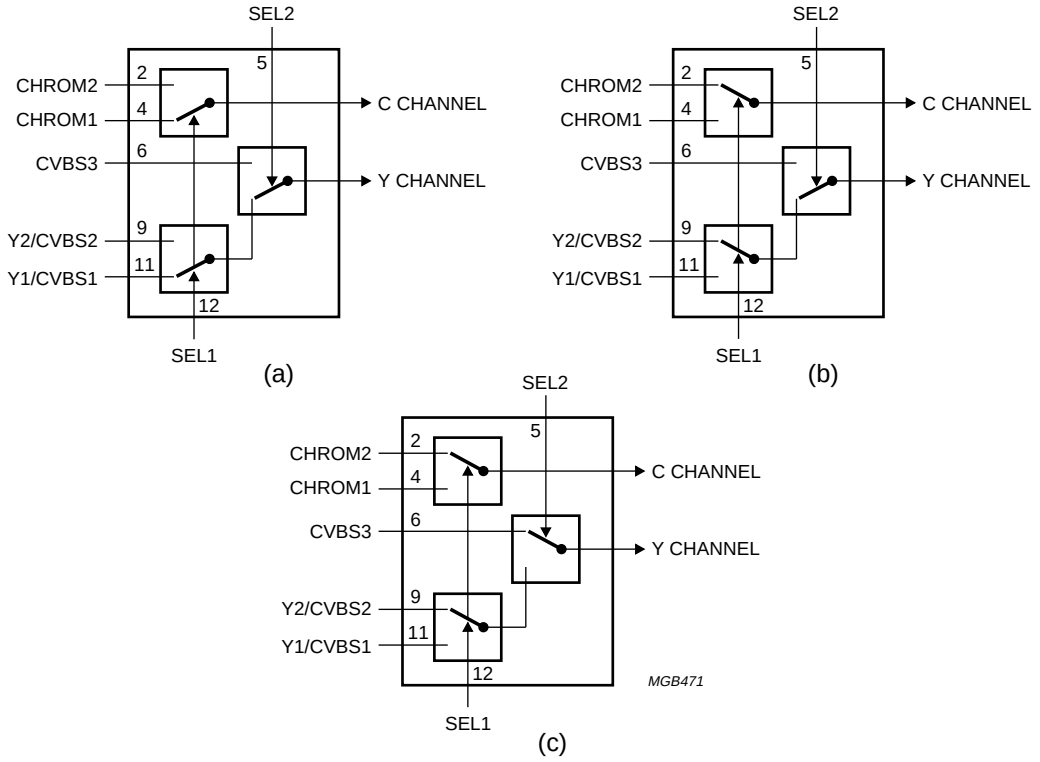



Fig.3 Video inputs selector.

**Table 1** Video input selection

| SEL1 | SEL2 | Y-CHANNEL | C-CHANNEL | FIGURE 3 |
|---|---|---|---|---|
| 0 | X[1] | Y1/CVBS1 | CHROM1 | (a) |
| 1 | 0 | Y2/CVBS2 | CHROM2 | (b) |
| 1 | 1 | CVBS3 | CHROM2 | (c) |

**Note**

1. X = don't care.

**Table 2** AGC output current

| $\overline{PWE}$ | GATE A | DIGITAL OUTPUT | $I_{AGC}$ |
|---|---|---|---|
| 0 | 0 | output < 255 | 0 μA |
| | | output > 255 | +540 μA |
| 0 | 1 | output < 0 | +8 μA |
| | | 0 < output < 255 | –8 μA |
| | | output > 255 | +540 μA |
| 1 | 0 | X[1] | 0 μA |
| 1 | 1 | output < 0 | +8 μA |
| | | 0 < output < 255 | –8 μA |

**Note**

1. X = don't care.

**Table 3** CLAMP output current

| CLAMP | GATE B | DIGITAL OUTPUT | $I_{CLAMP}$ |
|---|---|---|---|
| C | 1 | output < 128 | +54 μA |
| | | output > 128 | –54 μA |
| X[1] | 0 | X[1] | 0 μA |
| Y | 1 | output < 64 | +54 μA |
| | | 64 < output | –54 μA |

**Note**

1. X = don't care.

**Table 4** OFY and OFC input coding

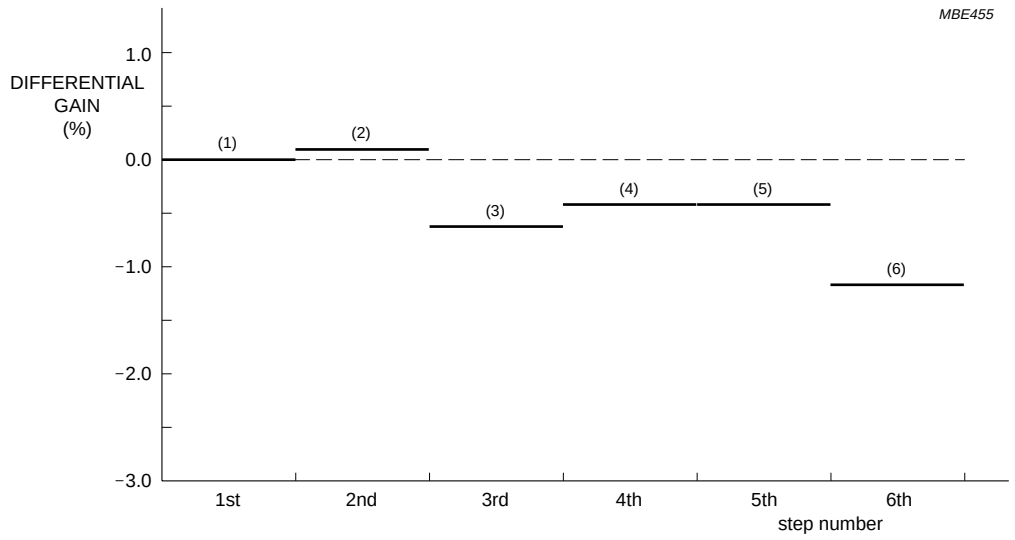
| OFY (or OFC) | Y0 to Y7 (or C0 TO C7) |
|---|---|
| 0 | active, twos complement |
| 1 | high impedance |
| open circuit[1] | active, binary |

**Note**

1. Use C ≥ 10 pF to DGND.

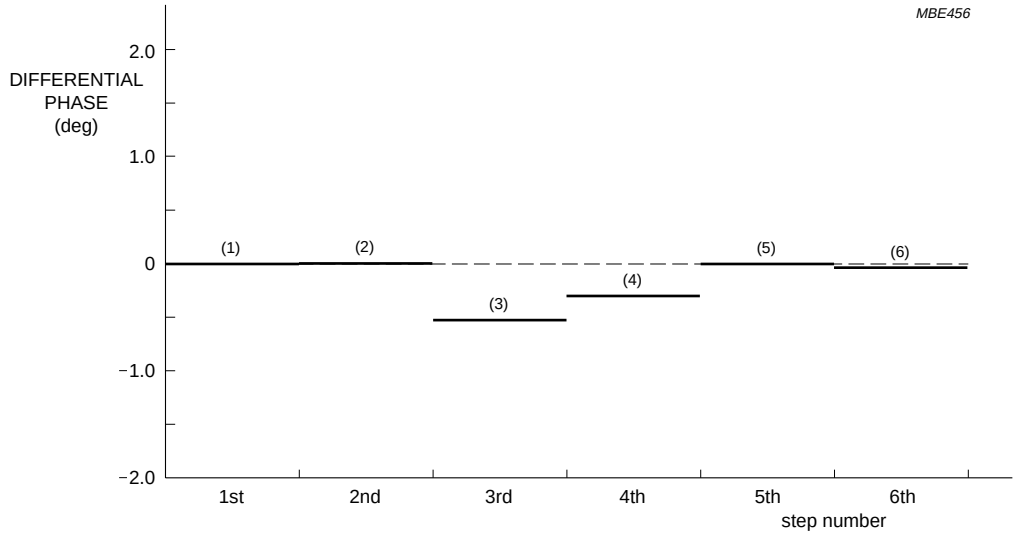
**Table 5** Output coding and ANOUTY (or ANOUTC) voltage (typical values)

| STEP | $V_I$ | BINARY OUTPUTS | | | | | | | | TWOS COMPLIMENT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Underflow | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 2.6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| . | – | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| . | – | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| 254 | – | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 255 | 3.6 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Overflow | – | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |




(1) = 0.00; (2) = 0.09; (3) = –0.63; (4) = –0.45; (5) = –0.45; (6) = –1.23.
Differential gain = max. (2) – min. (6) = 1.32%.

Fig.4 Typical differential gain result on VM700A.




(1) = 0.00; (2) = 0.03; (3) = –0.53; (4) = –0.32; (5) = 0.01; (6) = –0.08.
Differential phase = max. (2) – min. (3) = 0.56 deg.

Fig.5 Typical differential phase result on VM700A.

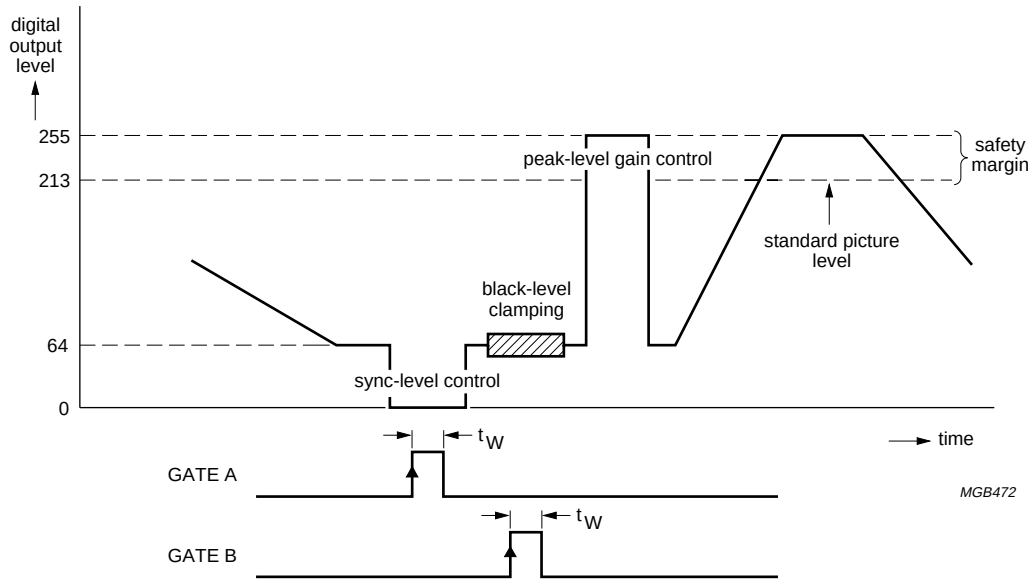



Fig.6 Control mode Y channel.

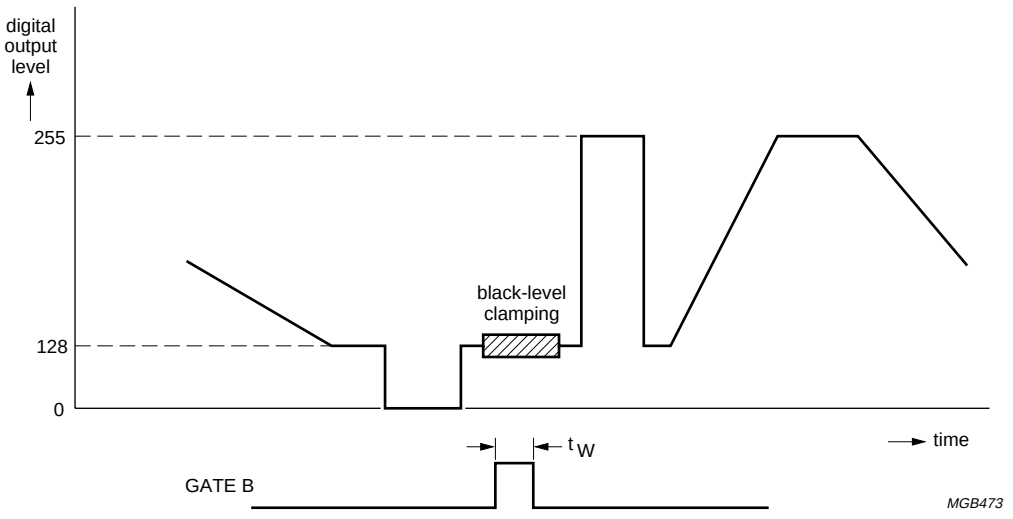
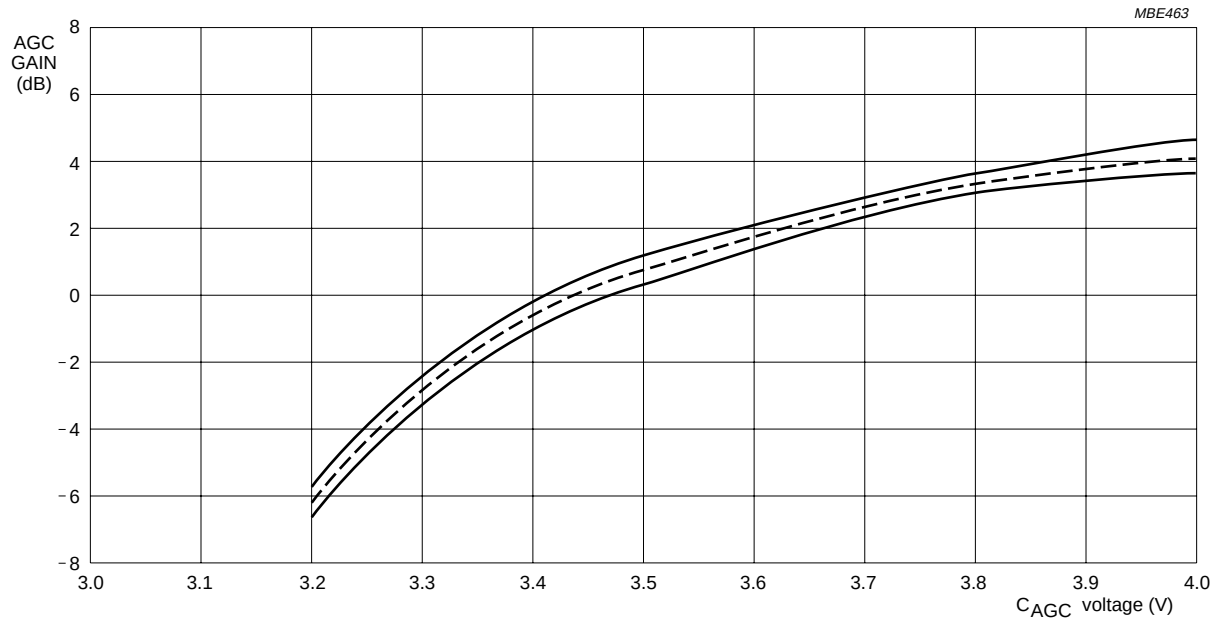



Fig.7 Control mode C-channel.




Dotted line: Typical curve ($T_{amb}$ = 25 °C; $V_{CC}$ = 5 V).
Full line: Maximum envelope ($T_{amb}$ = 0 to 70 °C; $V_{CC}$ = 4.75 to 5.25 V).

Fig.8 AGC behaviour as a function temperature and supply voltage for ANOUTY output; $f_i$ = 4.43 MHz, $V_i$ = 0 dB.

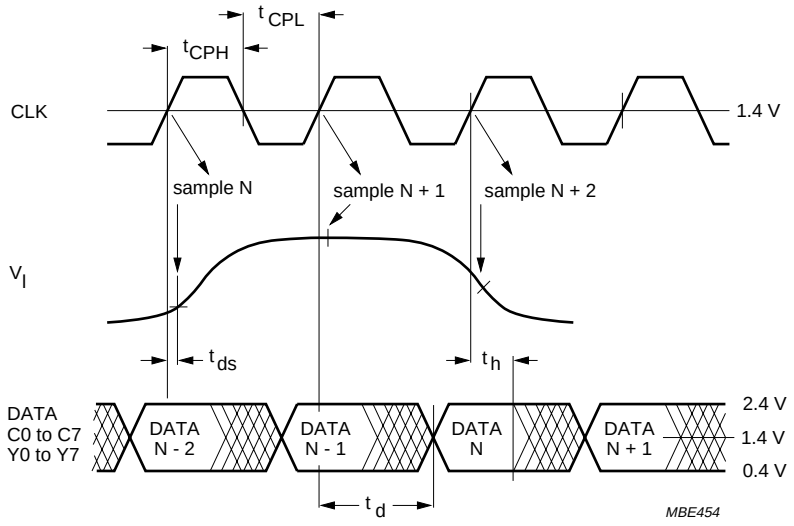
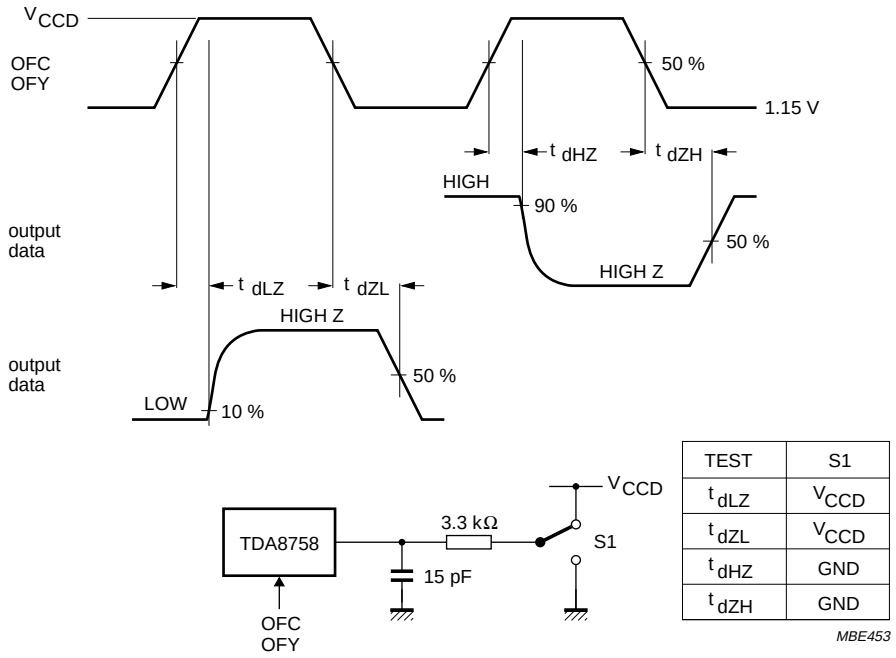



Fig.9 Timing diagram.

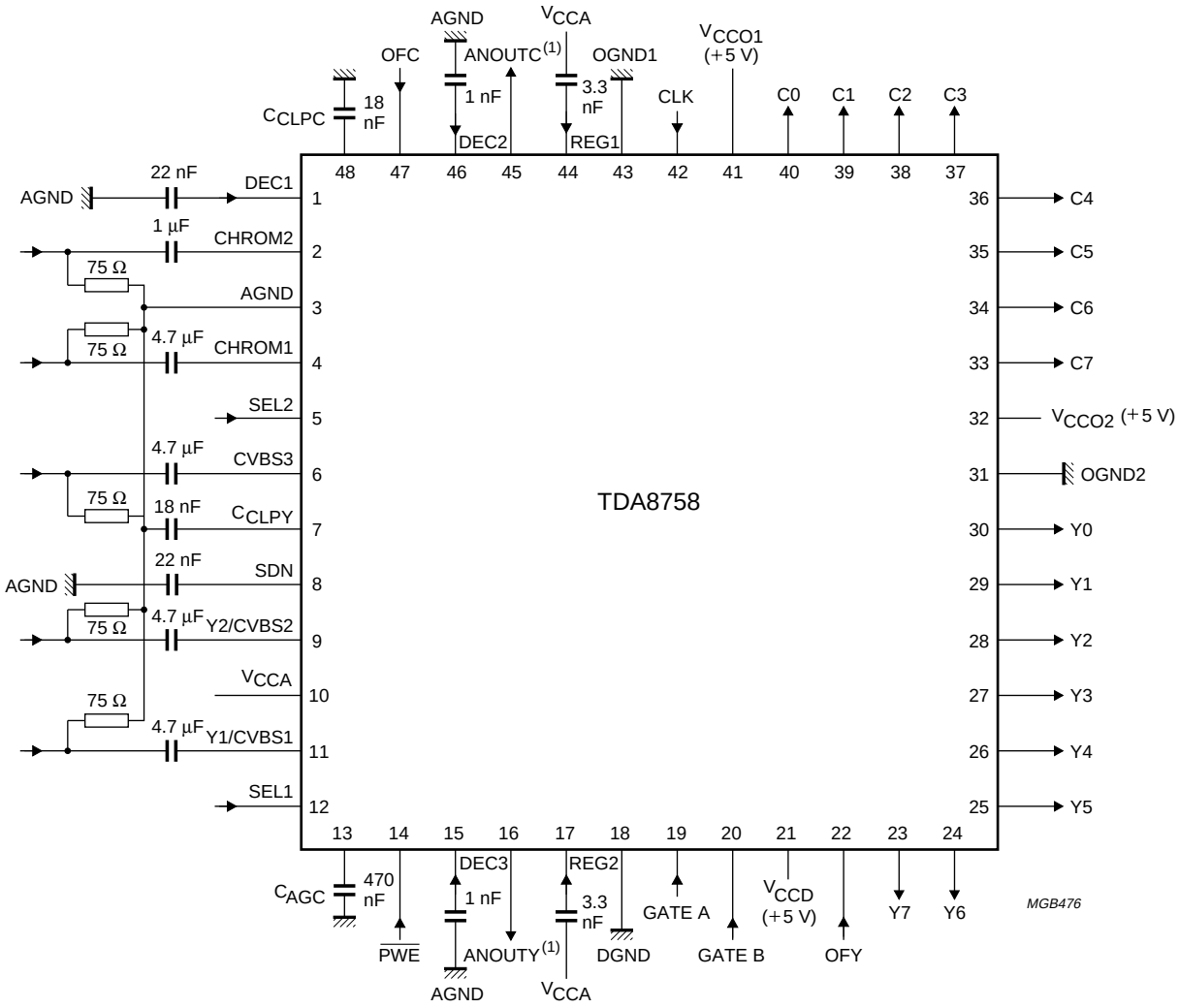



| TEST | S1 |
|---|---|
| $t_{dLZ}$ | $V_{CCD}$ |
| $t_{dZL}$ | $V_{CCD}$ |
| $t_{dHZ}$ | GND |
| $t_{dZH}$ | GND |

$f_{OFC} = f_{OFY} = 100$ kHz.

Fig.10 Timing diagram and test conditions of 3-state output delay time.

## APPLICATION INFORMATION




(1) It is recommended that pin 16 and pin 45 are not loaded in order to avoid any distortion.

Fig.11 Application diagram.

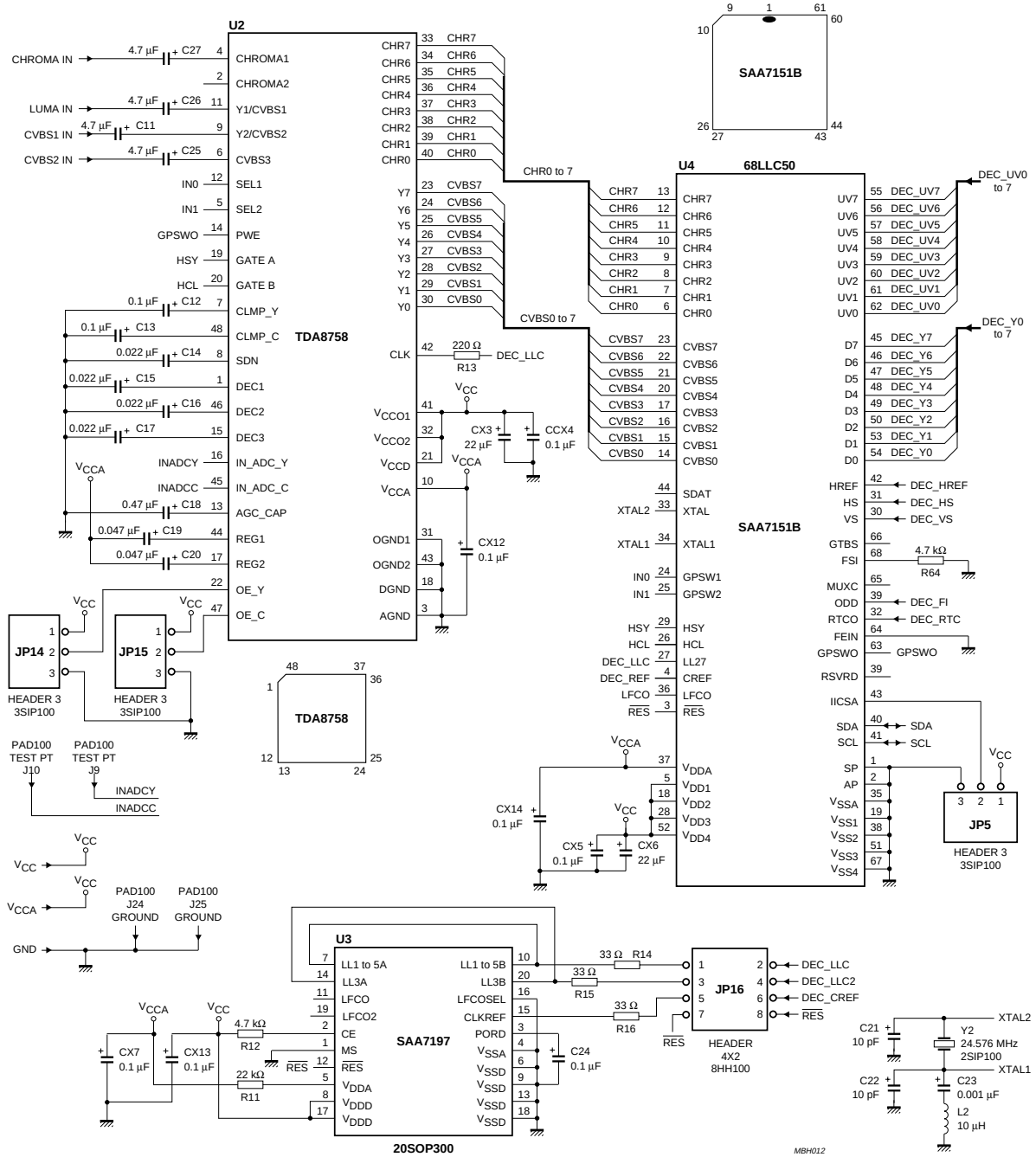
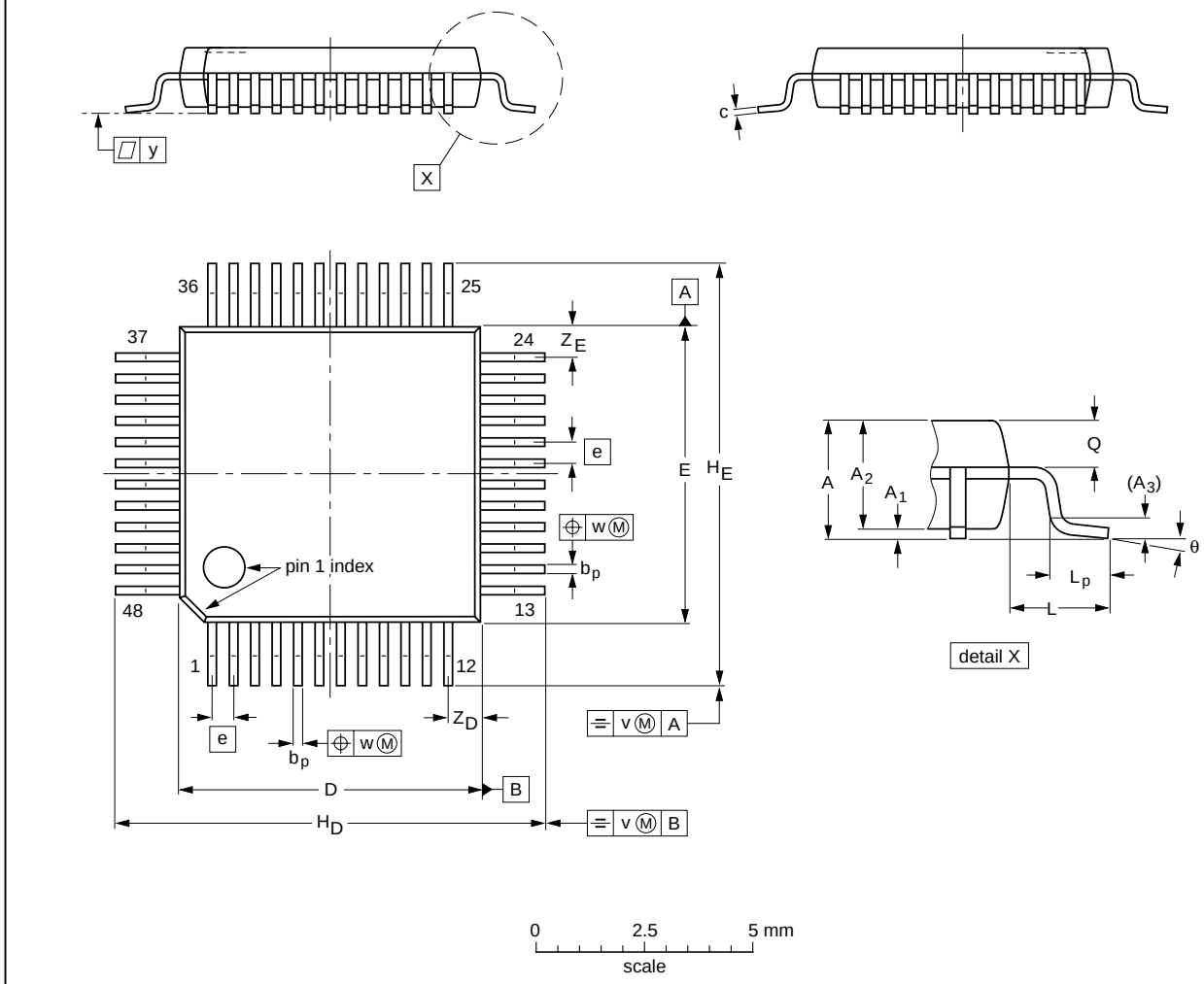



Fig.12 Example of system application (DPC71 evaluation board).

## PACKAGE OUTLINE

**LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm** **SOT313-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | Q | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.60 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 7.1<br>6.9 | 7.1<br>6.9 | 0.5 | 9.15<br>8.85 | 9.15<br>8.85 | 1.0 | 0.75<br>0.45 | 0.69<br>0.59 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT313-2 | | | | | | ~~93-06-15~~<br>94-12-19 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

### Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

**Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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**NOTES**

**NOTES**

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**Argentina:** IEROD, Av. Juramento 1992 - 14.b, (1428)
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